

TITLE OF THE INVENTION

Semiconductor Device

BACKGROUND OF THE INVENTION

Field of the Invention

5 The present invention relates to a semiconductor device with field-effect transistors.

Description of the Background Art

10 Conventionally, semiconductor devices using field-effect transistors have been manufactured. One field-effect transistor is provided in an element formation region surrounded by an element isolation part when viewed in the direction perpendicular to the main surface of a semiconductor substrate in such semiconductor devices. A single P-channel type transistor, for example, is provided in the element formation region and no other elements are provided in this structure.

15 It is necessary to individually separate transistors by means of an element isolation part in a semiconductor device having a structure that only a single field-effect transistor is formed in an element formation region as described above. Therefore, the area of the semiconductor device cannot be reduced in the direction parallel to the main surface of the semiconductor substrate.

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SUMMARY OF THE INVENTION

 It is an object of the present invention to provide a semiconductor device having a structure capable of achieving miniaturization of elements in a surface parallel to the main surface of a semiconductor substrate.

25 A semiconductor device according to the present invention includes: an element isolation part surrounding one element formation region when viewed in the direction perpendicular to a main surface of a semiconductor substrate and electrically isolating the one element formation region from another element formation regions; and a plurality of elements provided in the element formation region. The plurality of elements includes a first field-effect transistor and a second field-effect transistor functioning as high side switches of a latch circuit. The semiconductor device is utilized in the state where a lower side of one of the first field-effect transistor and

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the second field-effect transistor is completely depleted. The first field-effect transistor and the second field-effect transistor share a source region or a drain region.

5 With this configuration, it becomes possible to reduce the area of the element formation region where the high side switch of the latch circuit is formed. Accordingly, it becomes possible to miniaturize the semiconductor device.

10 A semiconductor device according to a second aspect of the present invention includes: a first field-effect transistor having a channel region of a first conductive type; and a second field-effect transistor having a channel region of a second conductive type which is a conductive type opposite to the first conductive type.

15 Further, in the semiconductor device, the gate electrode of the first field-effect transistor and the drain electrode of the second field-effect transistor are integrally formed of the same conductive layer and extend in sequence in a predetermined direction in a linear manner. Further, in the semiconductor device, the source electrode of the first field-effect transistor and the source electrode of the second field-effect transistor are integrally formed of the same conductive layer and extend in sequence in a
20 predetermined direction in a linear manner.

Further, the difference in potential between the source electrode of the first field-effect transistor and the drain electrode of the second field-effect transistor is approximately the same as the difference in potential between the gate electrode and the source electrode of the first field-effect
25 transistor.

Further, the punch through voltage between the impurity diffusion region of the second conductive type beneath the drain electrode of the second field-effect transistor and the impurity diffusion region of the second conductive type beneath the gate electrode of the first field-effect transistor is greater than the difference in potential between the source electrode of the first field-effect transistor and the drain electrode of the second field-effect transistor.
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With this configuration, the distance between the first field-effect

transistor and the second field-effect transistor can be extremely small. Therefore, the area of the element formation region can be reduced.

The foregoing and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a diagram for describing a structure of a semiconductor device according to a first embodiment;

Fig. 2 is a circuit diagram of the semiconductor device according to the first embodiment;

Fig. 3 is a diagram for describing a depletion layer formed when the semiconductor device according to the first embodiment operates;

Fig. 4 is a diagram for describing a depletion layer formed when the semiconductor device according to the first embodiment operates;

Fig. 5 is a diagram for describing a structure of a semiconductor device according to a second embodiment;

Fig. 6 is a circuit diagram of the semiconductor device according to the second embodiment;

Fig. 7 is a diagram for describing a depletion layer formed when a semiconductor device according to a third embodiment operates;

Fig. 8 is a diagram for describing a depletion layer formed when the semiconductor device according to the third embodiment operates;

Fig. 9 is a circuit diagram of the semiconductor device according to the third embodiment;

Figs. 10 and 11 are diagrams for describing a structure of a semiconductor device according to a fourth embodiment;

Fig. 12 is a circuit diagram of the semiconductor device according to the fourth embodiment; and

Figs. 13 to 16 are diagrams for describing structures of semiconductor devices according to fifth to eighth embodiments, respectively.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Hereinafter, semiconductor devices according to embodiments of the present invention will be described with reference to the drawings.

First Embodiment

5 First, a structure of a semiconductor device according to a first embodiment will be described with reference to Figs. 1 to 4. As shown in Fig. 1, the semiconductor device according to the present embodiment includes a P⁻-type semiconductor substrate 1, and an N⁻-type epitaxial layer 2 formed in the range from the main surface of P⁻-type semiconductor substrate 1 to a predetermined depth. Further, the semiconductor device
10 according to the present embodiment includes a P⁺-type impurity diffusion region 3 formed in the range from the main surface of P⁻-type semiconductor substrate 1 to a predetermined depth and a P⁺-type impurity diffusion region 3a formed on the upper portion of P⁺-type impurity diffusion region 3 inside N⁻ epitaxial layer 2.

15 Further, a P⁻-type impurity diffusion region 4 is formed adjacent to the side of P⁺-type impurity diffusion region 3a. Further, an N⁺-type impurity diffusion region 5 is formed at a predetermined distance away from the side of P⁻-type impurity diffusion region 4. A P⁺-type impurity diffusion region 6 is formed adjacent to N⁺-type impurity diffusion region 5.
20 A source electrode V_{aa} electrode 8 is provided so as to be connected to N⁺-type impurity diffusion region 5 and P⁺-type impurity diffusion region 6, respectively.

Further, a P⁻-type impurity diffusion region 11 is formed at a distance away from the side of P⁺-type impurity diffusion region 6.
25 Further, a gate electrode V_{g1} 9, having a region between P⁺-type impurity diffusion region 6 and P⁻-type impurity diffusion region 11 as a channel region, is formed above semiconductor substrate 1. Further, a P⁺-type impurity diffusion region 7 is formed on a region inside P⁻-type impurity diffusion region 11. A drain electrode V_{d1} 10 is connected to the upper
30 surface of P⁺-type impurity diffusion region 7.

Further, a P⁺-type impurity diffusion region 12 is formed at a predetermined distance away from the side of P⁻-type impurity diffusion region 11. A gate electrode V_{g1} 13 is formed so as to have a region between

P⁺-type impurity diffusion region 12 and P⁻-type impurity diffusion region 11 as a channel region. An N⁺-type impurity diffusion region 14 is formed adjacent to P⁺-type impurity diffusion region 12. Further, a P⁺-type impurity diffusion region 16 is formed adjacent to N⁺-type impurity diffusion region 14. Further, a source electrode V_{sd} 15 is formed so as to bring into contact with P⁺-type impurity diffusion region 12, N⁺-type impurity diffusion region 14 and P⁺-type impurity diffusion region 16, respectively.

Further, a P⁻-type impurity diffusion region 19 is formed at a predetermined distance away from P⁺-type impurity diffusion region 16. A gate electrode V_{g2} 17 is formed so as to have a region between P⁻-type impurity diffusion region 19 and P⁺-type impurity diffusion region 16 as a channel region. Further, a P⁺-type impurity diffusion region 18 is formed on a region inside P⁻-type impurity diffusion region 19. Further, a drain electrode V_{d2} 20 is connected to P⁺-type impurity diffusion region 18. A P⁺-type impurity diffusion region 22 is formed at a predetermined distance away from P⁻-type impurity diffusion region 19. A gate electrode V_{g2} 21 is formed so as to have a region between P⁺-type impurity diffusion region 22 and P⁻-type impurity diffusion region 19 as a channel region.

Further, an N⁺-type impurity diffusion region 23 is provided adjacent to P⁺-type impurity diffusion region 22. A source electrode V_{sd} 24 is connected to P⁺-type impurity diffusion region 22 and N⁺-type impurity diffusion region 23, respectively. Further, a P⁻-type impurity diffusion region 25 is formed at a predetermined distance away from the side of N⁺-type impurity diffusion region 23. Further, P⁻-type impurity diffusion region 25 is located adjacent to P⁺-type impurity diffusion region 3a. Further, P⁺-type impurity diffusion region 3a is provided with P⁺-type impurity diffusion region 3 in its lower side. It is noted that P⁺-type impurity diffusion region 3a is connected to a ground electrode.

The left side of the above described semiconductor device, with N⁺-type impurity diffusion region 14 serving as the border, forms a field PMOS (P Channel Metal Oxide Semiconductor) 1 and the right side thereof forms a field PMOS 2. It is noted that a field PMOS (NMOS) means a MOS

transistor having a gate insulating film formed of a LOCOS (LOCAl Oxidation of Silicon) field oxide film. It is noted that gate insulating films formed between gate electrodes and the semiconductor substrate are not shown in the drawings of the present specification.

5 Field PMOS 1 and field PMOS 2, as high side switches of a latch circuit, share P⁺-type impurity diffusion region 12, N⁺-type impurity diffusion region 14 and P⁺-type impurity diffusion region 16, which are connected to source electrode V_{dd} 15, in the above described semiconductor device. Therefore, the area of the element formation region in the
10 direction parallel to the main surface of semiconductor substrate 1 is reduced in comparison with the prior art. As a result, the semiconductor device can be miniaturized. It is noted that a high side switch means a switch connected to a power supply electrode (high potential side) in the case where two switch elements are connected in series between the power
15 supply electrode (high potential side) and a ground electrode (low potential side).

 It is noted that Fig. 2 is a diagram showing a way of use in the semiconductor device shown in Fig. 1 as a circuit (latch circuit). In addition, the high side of the latch circuit is the side connected to the
20 electrode to which voltage V_{dd} of the latch circuit shown in Fig. 2 is applied, and field PMOS 1, field PMOS 2 and field PMOS 3 correspond to the high side switches in the latch circuit of the present embodiment.

 The dotted line in Fig. 3 shows a depletion layer formed in the case where a voltage equal to or more than threshold voltage is applied to gate
25 electrode V_{g2} 17, 21 so that the voltage of drain electrode V_{d2} 20 becomes V_{dd} and, also, a voltage equal to or less than threshold voltage is applied to gate electrode V_{g1} 9, 13 so that the voltage of drain electrode V_{d1} 10 becomes 0. Further, the dotted line in Fig. 4 shows a depletion layer formed in the case where a voltage equal to or more than threshold voltage is applied to gate
30 electrode V_{g1} 9, 13 so that the voltage of drain electrode V_{d1} 10 becomes V_{dd} and, also, a voltage equal to or less than threshold voltage is applied to gate electrode V_{g2} 17, 21 so that the voltage of drain electrode V_{d2} 20 becomes 0.

 As can be seen from Figs. 3 and 4, the depletion layer extends from

P⁻-type semiconductor substrate 1 and P⁻-type impurity diffusion regions 4, 6, 11, 12, 16, 19, 22 and 25, respectively, when the latch circuit is in the off-state; thereby, N⁻-type epitaxial layer 2 is completely depleted.

Accordingly, the surface electrical field of N⁻-type epitaxial layer 2 is relaxed.

Further, the depletion layer extending from P⁻-type semiconductor substrate 1 does not reach P⁻-type impurity diffusion regions 4, 6, 11, 12, 16, 19, 22 and 25. Such an effect is an effect accompanying the structure of relaxing the surface electrical field referred to as DOUBLE RESURF, and is described in Japanese Patent Laying-Open No. 10-4143. The withstand voltage of the element becomes a one-dimensional withstand voltage in the direction perpendicular to the main surface of the semiconductor substrate if the DOUBLE RESURF condition for relaxing the surface electrical field is satisfied. Accordingly, the withstand voltage of the element is determined by the withstand voltage between P⁻-type semiconductor substrate 1 and N⁻-type epitaxial layer 2.

It is therefore possible to easily change the withstand voltage by adjusting the respective concentrations of the impurities in P⁻-type semiconductor substrate 1 and N⁻-type epitaxial layer 2. It is therefore possible to make the withstand voltage equal to or more than 1000 V. As a result, a logic signal can be converted into a digital signal of approximately 1000 V according to the latch circuit of the present embodiment. Therefore, the latch circuits of the present embodiment, as well as of the respective embodiments described below, are considerably useful as drive circuits in regard to electrostatic induction force or piezoelectric force that become drive sources of MEMS (Micro Electro Mechanical Systems).

Second Embodiment

Next, a structure of a semiconductor device according to a second embodiment will be described with reference to Fig. 5. The structure of the semiconductor device according to the second embodiment is approximately similar to that of the semiconductor device, shown in Fig. 1, of the first embodiment. However, the structure of the semiconductor device according to the present embodiment differs from that of the

semiconductor device shown in Fig. 1 of the first embodiment only in that an N⁺-type impurity diffusion region 28 is formed inside P⁺-type impurity diffusion region 18.

Accordingly, a P-channel IGBT (Insulated Gate Bipolar Transistor),
5 instead of field PMOS 2, is formed in the right side of the semiconductor device of the present embodiment with source electrode V_{dd} 15 as the border. A forward bias (positive bias) generates between P⁺-type impurity diffusion region 18 and N⁺-type impurity diffusion region 28 in this P-channel IGBT; thereby, an NPN transistor having N⁺-type impurity diffusion region 28 as
10 an emitter electrode functions. Thereby, the current is amplified to be multiplied by hFE by means of the NPN transistor.

Field PMOS 1 and the field P-channel IGBT, as high side switches of a latch circuit, also share P⁺-type impurity diffusion region 12, N⁺-type impurity diffusion region 14 and P⁺-type impurity diffusion region 16,
15 which are connected to source electrode V_{dd} 15, in the above described semiconductor device of the present embodiment. Therefore, the area of the element formation region in a plane parallel to the main surface of semiconductor substrate 1 can be reduced. As a result, it is possible to miniaturize the semiconductor device.

Further, the on-resistance of the P-channel IGBT is sufficiently small; therefore, it is not necessary to provide PMOS 3 for output, as shown in Fig. 2. Accordingly, the area of the element formation region in the direction parallel to the main surface of semiconductor substrate 1 can be further reduced in comparison with the semiconductor device according to
25 the first embodiment.

It is noted that Fig. 6 shows a circuit diagram indicating the way of use of the structure of the semiconductor device shown in Fig. 5 in the latch circuit.

Third Embodiment

30 Next, a structure of a semiconductor device according to the present embodiment will be described with reference to Fig. 7.

The structure of the semiconductor device according to the present embodiment is approximately similar to that of the semiconductor device

according to the first embodiment shown in Fig. 1; therefore, only the parts of the structure which is different from those in the semiconductor device according to the first embodiment will be described. The structure of field PMOS 2 in the left side region of the semiconductor device with source electrode V_{dd} 15 as the border is exactly the same as the structure of field PMOS 1 of the first embodiment. The structure of the semiconductor device of the present embodiment differs from the structure of the semiconductor device of the first embodiment in the following manner.

A P⁻-type impurity diffusion region 31 is formed in the vicinity of N⁺-type impurity diffusion region 14. A P⁺-type impurity diffusion region 32 is formed adjacent to P⁻-type impurity diffusion region 31. Further, an N⁺-type impurity diffusion region 33 is formed inside P⁺-type impurity diffusion region 32. An electrode V_{out} 38 is connected to both P⁺-type impurity diffusion region 32 and N⁺-type impurity diffusion region 33. Further, a P⁺-type impurity diffusion region 34 is formed at a predetermined distance away from the side of P⁺-type impurity diffusion region 32.

An N⁺-type impurity diffusion region 35 is formed inside P⁺-type impurity diffusion region 34. Further, a gate electrode V_{g4} 39 is provided so as to have a region between P⁺-type impurity diffusion region 32 and P⁺-type impurity diffusion region 34 as a channel region. Further, drain electrode V_{out} 38 is connected to P⁺-type impurity diffusion region 32. Further, a drain electrode V_{out} 40 is connected to P⁺-type impurity diffusion region 34.

Further, a P⁻-type impurity diffusion region 30 is formed adjacent to P⁺-type impurity diffusion region 34. Further, an N⁺-type impurity diffusion region 37 is formed at a predetermined distance away from the side of P⁻-type impurity diffusion region 30. A source electrode V_{dd} 41 is connected to N⁺-type impurity diffusion region 37.

Field PMOS 2 and an NMOS (N Channel Metal Oxide Semiconductor) 4, as high side switches of a latch circuit, also share P⁺-type impurity diffusion region 12 and N⁺-type impurity diffusion region 14, which are connected to source electrode V_{dd} 15, as well as P⁺-type impurity

diffusion region 31 in the above described semiconductor device of the present embodiment. Accordingly, the area of the element formation region in a plane parallel to the main surface of semiconductor substrate 1 can be reduced. As a result, the semiconductor device can be miniaturized even by means of the semiconductor device according to the present
5 embodiment.

In addition, the mobility (moving speed) of charge is three times greater in an NMOS in comparison with that in a PMOS. Therefore, the area of an NMOS in the direction parallel to the main surface of
10 semiconductor substrate 1 can be reduced in comparison with a PMOS.

Further, the dotted line in Fig. 7 shows a depletion layer formed in the case where a voltage equal to or less than threshold voltage is applied to gate electrode V_{g2} 9, 13 so that the voltage of drain electrode V_{d2} 10 becomes 0 and, also, a voltage equal to or more than threshold voltage is
15 applied to gate electrode V_{g4} 39 so that the voltage of drain electrode V_{out} 38, 40 becomes V_{dd} .

In addition, Fig. 8 shows the structure of the same semiconductor device shown in Fig. 7. The dotted line in Fig. 8 shows a depletion layer formed in the case where a voltage equal to or more than threshold voltage
20 is applied to gate electrode V_{g2} 9, 13 so that the voltage of drain electrode V_{d2} 10 becomes V_{dd} and, also, a voltage equal to or less than the threshold voltage is applied to gate electrode V_{g4} 39 so that the voltage of drain electrode V_{out} becomes 0.

It is noted that Fig. 9 shows a circuit diagram indicating the way of
25 use of the semiconductor device shown in Figs. 7 and 8 in a circuit (latch circuit). This latch circuit differs from that of the circuit diagram of the semiconductor device according to the first or second embodiment in that a Zener diode is provided to protect gate electrode V_{g4} 39 of NMOS 4.

Further, although field PMOS 2 is not shown in Figs. 7 and 8, field
30 PMOS 2, field PMOS 1 and NMOS 4 may share P⁺-type impurity diffusion region 12 and N⁺-type impurity diffusion region 14, which are connected to source electrode V_{dd} 15, as well as P⁺-type impurity diffusion region 31.
Fourth Embodiment

Next, a semiconductor device according to a fourth embodiment will be described with reference to Figs. 10 to 12. The structure of the semiconductor device according to the fourth embodiment differs from that of the semiconductor device according to the third embodiment shown in Figs. 7 and 8 only in that NMOS 4 is a field NMOS. A voltage of 0 is applied to a gate electrode V_{d2} 39 of this field NMOS. Further, a voltage of 0 is also applied to drain electrode V_{d2} 10 of field PMOS 2. The broken line in Fig. 10 shows a depletion layer formed at this time.

Further, voltage V_{dd} is applied to drain electrode V_{d2} 10 of field PMOS 2 and voltage V_{dd} is applied to gate electrode V_{d2} 39 of the field NMOS in Fig. 11. The dotted line in Fig. 11 shows a depletion layer formed at this time. In addition, Fig. 12 shows a circuit diagram indicating the way of use of the semiconductor device shown in Figs. 10 and 11 in a circuit.

Field PMOS 2 and the field NMOS, as high side switches of a latch circuit, also share P⁺-type impurity diffusion region 12 and N⁺-type impurity diffusion region 14, which are connected to source electrode V_{dd} 15, in the above described semiconductor device of the present embodiment. Further, N⁺-type impurity diffusion region 14 connected to source electrode V_{dd} 15 and P⁻-type impurity diffusion region 31 connected to drain electrode V_{out} 38 are provided adjacent to each other in the semiconductor device of the present embodiment. Accordingly, the area of the semiconductor device in the direction parallel to the main surface of semiconductor substrate 1 can be reduced. As a result, the structure of the semiconductor device of the present embodiment also allows miniaturization of the element formation region.

It is noted that, as shown in Fig. 12, the latch circuit of the present embodiment has a field NMOS in place of the NMOS of the latch circuit, shown in Fig. 9, of the third embodiment. A field NMOS has a withstand voltage higher than that of an NMOS. Accordingly, a Zener diode as used in the latch circuit so as to protect the NMOS, as shown in Fig. 9, is not used herein.

Fifth Embodiment

A semiconductor device according to a fifth embodiment will be described with reference to Fig. 13. Fig. 13 is a diagram showing a structure that the planar positions of field PMOS 2 and NMOS 4 of the semiconductor device according to the third embodiment shown in Figs. 7 to 9 are changed. It is noted that Fig. 13 is a diagram schematically showing the vicinity of the main surface of the semiconductor substrate when viewed in the direction perpendicular to the main surface of semiconductor substrate 1.

The respective parts in the structure shown in Fig. 13 to which reference symbols are attached have the same functions as the respective parts in the structure shown in Figs. 7 to 9 to which the same reference symbols are attached. In other words, the semiconductor device shown in Fig. 13 and the semiconductor device shown in Figs. 7 to 9 have the same functions and differ from each other only in the arrangement of the respective parts.

As shown in Fig. 13, gate electrode 39 of NMOS 4 and drain electrode 10 of field PMOS 2 are integrally formed of the same conductive layer and sequentially extend in a predetermined direction in a linear manner. Further, source electrodes 15, 41 of NMOS 4 and source electrode 8, 15 of field PMOS 2 are integrally formed of the same conductive layer and sequentially extend in a predetermined direction in a linear manner.

The difference in potential between source electrodes 15, 41 of NMOS 4 and drain electrode 10 of field PMOS 2 is approximately the same as the difference in potential between gate electrode 39 and source electrodes 15, 41 of NMOS 4.

Therefore, the semiconductor device of the present embodiment is formed so that the punch through voltage between P⁺-type impurity diffusion region 7 beneath drain electrode 10 of field PMOS 2 and P⁺-type impurity diffusion regions 32, 34 beneath gate electrode 39 of NMOS 4 becomes greater than the difference in potential between source electrodes 15, 41 of NMOS 4 and drain electrode 10 of field PMOS 2 in the case where NMOS 4 and field PMOS 2 are formed in the arrangement shown in Fig. 13.

With this arrangement, the generation of punch through between P⁺-

type impurity diffusion region 7 beneath drain electrode 10 of field PMOS 2 and P⁺-type impurity diffusion regions 32, 34 beneath gate electrode 39 of NMOS 4 can be suppressed even in the case where NMOS 4 and field PMOS 2 are provided in close proximity to each other.

5 Sixth Embodiment

Next, a structure of a semiconductor device according to the present embodiment will be described with reference to Fig. 14.

The structure of the semiconductor device of the present embodiment is approximately similar to that of the semiconductor device, shown in Fig. 1, in the first embodiment. However, the structure of the semiconductor device of the present embodiment differs from that of the semiconductor device shown in Fig. 1 in that N⁺-type impurity diffusion regions 5, 14 and 23 are provided so as to reach very deep positions and so as to spread over a very wide region in comparison with N⁺-type impurity diffusion regions 5, 14 and 23 of the semiconductor device according to the first embodiment.

Thus, N⁺-type impurity diffusion regions 5, 14 and 23 are formed deeply and widely; thereby, N⁺-type impurity diffusion regions 5, 14 and 23 are located between P⁺-type semiconductor substrate 1 and P⁺-type impurity diffusion regions 6, 12, 16 and 22. Thereby, an effect can be obtained in that the operation of a parasitic V-PNP Tr formed of P⁺-type semiconductor substrate 1, N⁻-type impurity diffusion region 2 and P⁺-type impurity diffusion regions 6, 12, 16 and 22 can be suppressed.

Seventh Embodiment

Next, a structure of a semiconductor device according to the present embodiment will be described with reference to Fig. 15.

The structure of the semiconductor device according to the present embodiment is approximately similar to that of the semiconductor device, shown in Fig. 1, of the first embodiment. However, the structure of the semiconductor device according to the present embodiment shown in Fig. 15 differs from that of the semiconductor device shown in Fig. 1 in regard to the following points.

An N⁺-type impurity diffusion region 45 is formed so as to bring into contact with the lower surfaces of N⁺-type impurity diffusion region 14, P⁺-

type impurity diffusion region 12 and P⁺-type impurity diffusion region 16. Further, N⁺-type impurity diffusion region 46 is formed so as to bring into contact with the lower surfaces of N⁺-type impurity diffusion region 22 and N⁺-type impurity diffusion region 23. In addition, an N⁺-type impurity
5 diffusion region 47 is formed so as to bring into contact with the lower surfaces of N⁺-type impurity diffusion region 5 and P⁺-type impurity diffusion region 6.

N⁺-type impurity diffusion regions 47, 45 and 46 are located between P⁺-type semiconductor substrate 1 and P⁺-type impurity diffusion regions 6,
10 12, 16 and 22 in the semiconductor device of the above described structure. With this structure, an effect can be obtained in that the operation of a parasitic V-PNP Tr formed of P⁺-type semiconductor substrate 1, N⁻-type impurity diffusion region 2 and P⁺-type impurity diffusion regions 6, 12, 16 and 22 can be suppressed.

15 Eighth Embodiment

Next, a structure of a semiconductor device according to the present embodiment will be described with reference to Fig. 16.

The structure of the semiconductor device according to the present invention is approximately similar to that of the semiconductor device
20 according to the first embodiment shown in Fig. 1. However, the semiconductor device according to the present embodiment differs from the semiconductor device shown in Fig. 1 in the following point.

An N⁺-type impurity diffusion region 51 is formed beneath P⁺-type impurity diffusion region 12, N⁺-type impurity diffusion region 14 and P⁺-
25 type impurity diffusion region 16 so as to straddle the borderline between N⁻-type epitaxial layer 2 and semiconductor substrate 1 having a P⁻-type impurity diffusion region. Further, an N⁺-type impurity diffusion region 50 is formed beneath N⁺-type impurity diffusion region 5 and P⁺-type impurity diffusion region 6. Further, an N⁺-type impurity diffusion region
30 52 is formed beneath N⁺-type impurity diffusion region 23 and P⁺-type impurity diffusion region 22.

N⁺-type impurity diffusion regions 50, 51 and 52 are located between P⁺-type semiconductor substrate 1 and P⁺-type impurity diffusion regions 6,

12, 16 and 22 in the above described semiconductor device. Thereby, an effect can be obtained in that the operation of a parasitic V-PNP Tr formed of P⁺-type semiconductor substrate 1, N⁻-type impurity diffusion region 2 and P⁺-type impurity diffusion regions 6, 12, 16 and 22 can be suppressed.

5 It is noted that two elements are formed inside the element isolation part in the semiconductor device of each of the above described embodiments and a structure is shown wherein the two elements share a source region. However, the semiconductor device of the present invention may be a semiconductor device having a structure that a plurality, three, or
10 more, of elements, wherein there is no limitation to two elements, shares a source region.

In addition, a structure that the impurity diffusion region shared by two elements is a source region is shown in the semiconductor device of each of the embodiments. However, an effect can be obtained in that the
15 area of the elements in the direction parallel to the main surface of the semiconductor substrate can be reduced even in the case where the semiconductor device of the present invention has a structure that the impurity diffusion region shared by the two elements is a drain region.

It is noted that reference symbols are attached in the drawings of each of the above described embodiments. Although the parts indicated by the same reference symbols have the same functions in each of the drawings, descriptions of the functions of corresponding parts are not
20 repeated in the embodiments.

In addition, although the following repeats the descriptions found in each of the embodiments, one of the features of the semiconductor device according to each of the first to eighth embodiments is that the
25 semiconductor device is utilized in the state where an area beneath one of the two high side switches of the latch circuit is completely depleted.

Although the present invention has been described and illustrated in detail, it is clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the spirit and scope of the present invention being limited only by the terms of the
30 appended claims.